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EXPLANATION OF IEEE/IEC LOGIC SYMBOLS FOR MEMORIES

1. INTRODUCTION

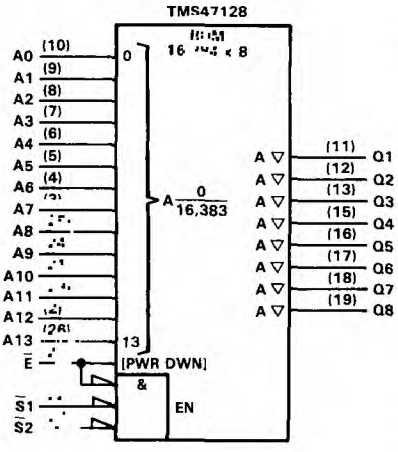
The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing *explicitly* the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

The current standards are IEC Publication 617-12, 1983, and ANSI/IEEE Standard 91-1984. Most of the data sheets in this data book include symbols prepared in accordance with these standards. The explanation that follows is necessarily brief and greatly condensed from the explanation given in the standards. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

2. EXPLANATION OF A TYPICAL SYMBOL FOR A STATIC MEMORY

The TMS47128 symbol will be explained in detail. This symbol includes almost all the features found in the ROMs, PROMs, and EPROMS.



The address inputs are arranged in the order of their assigned binary weights and the range of addresses are shown as $A\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The outputs affected by these addresses are designated by the letter A, as data inputs would also be if the device were a RAM.

The polarity indicator ◺ indicates that the external low level causes the internal 1-state (the active or asserted state) at an input or that the internal 1-state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol ○ .

The ▽ symbols indicate three-state outputs. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1-state, the outputs are enabled; when EN stands at its internal 0-state, the outputs stand at their high-impedance states. Sometimes the EN is a single input but in the illustrated case, it is the output of a three-input AND gate. All three inputs (pins 20, 22, and 27) are active low so if any one of them goes high, the outputs will be disabled. The upper one of these three inputs (pin 20) has another function. When nonstandard labels and explanatory labels are used within symbols, they are enclosed within square brackets. Here we find the label "[PWR DWN]". This is intended to indicate that if pin 20 is high, the memory will go to a low-power standby state.

3. THE BASICS

Section 3.1 illustrates the most common building blocks that are used in constructing symbols for memories. On the left are shown the symbols that specify the active levels for level-operated inputs, and the direction of active transition for dynamic inputs.

It is preferred to show all input lines on the left and all output lines on the right. When an exception is made to this left-to-right signal flow, an arrowhead is used to show the reverse signal flow.

Three symbols are shown that indicate 3-state, open-drain, and open-source outputs. If none of these are used, the output should be assumed to be totem-pole. The common control block is a point of placement for inputs that affect an array of elements.

The drawings on the right define the three forms of *dependency notation* used in this book. At an input (or output) that affects other inputs or outputs, a letter (G, C, or Z) is placed followed by a number. That same number is placed at the affected inputs and outputs. The letter G indicates that an AND relationship exists; if the affecting input stands at the 0-state, it imposes that 0-state on the affected input or output. The letter C indicates a control relationship, usually between a clock and a D (data) input. If the C input stands at its 0-state, the affected input is disabled. A D input is always an input to a storage element, which it either sets to the 1-state or resets to the 0-state, unless the D input is disabled to have no effect. Z dependency is used to transfer a signal from one place in a symbol to another, for example from the output at Z4 across to a terminal labeled "4", or from the output at Z5 back to the "5" where it serves as an input with no terminal attached.

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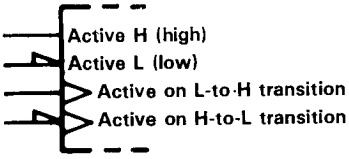
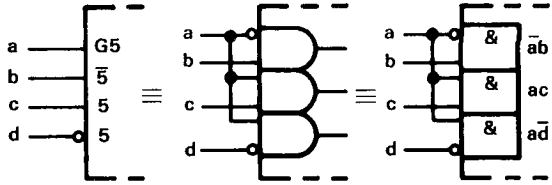
3.1 DIAGRAMATIC SUMMARY

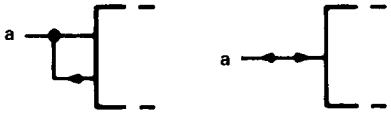
INPUTS



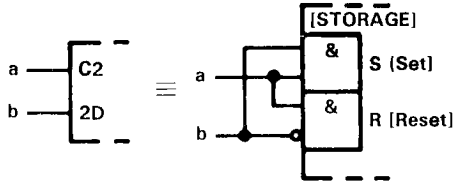
G (AND) DEPENDENCY



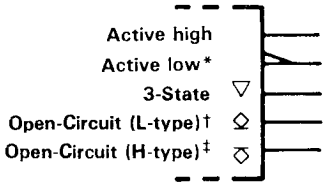
INPUT/OUTPUT



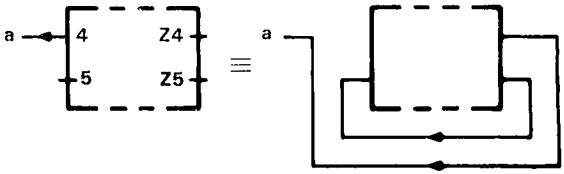
C (CONTROL) DEPENDENCY



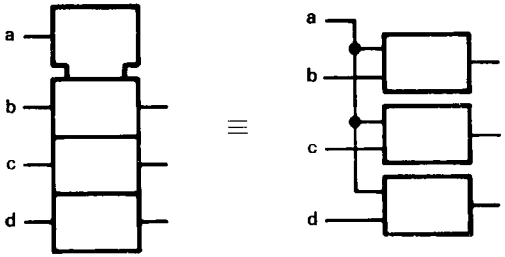
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



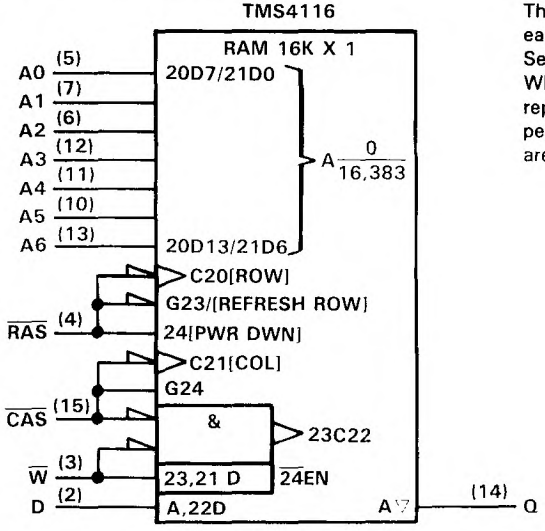
COMMON CONTROL BLOCK



*The active-low indicator may be used in combination with the 3-state and open-circuit indicators.
†L-types include N-channel open-drain and P-channel open-source outputs.
‡H-types include P-channel open-drain and N-channel open-source outputs.

4. EXPLANATION OF A TYPICAL SYMBOL FOR A DYNAMIC MEMORY

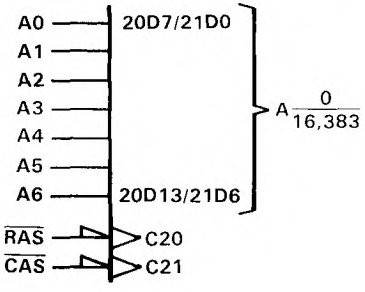
4.1 THE TMS4116 SYMBOL

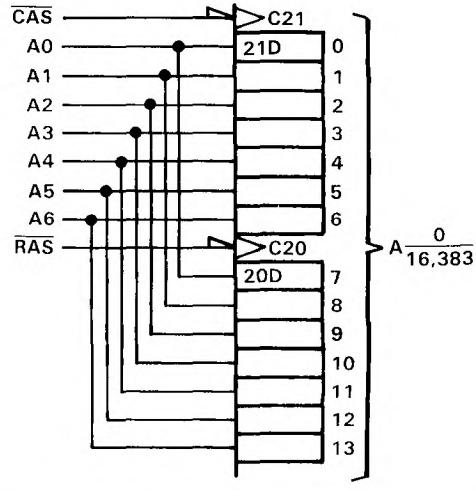


The TMS4116 symbol will be explained in detail for each operating function. The assumption is made that Sections 2 and 3 have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

4.2 ADDRESSING

The symbol above makes use of an abbreviated form to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.





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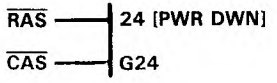
When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the seven address registers 7 through 13. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the seven address registers 0 through 6. The outputs of the address registers are the 14 internal address lines that select 1 of 16,384 cells.

4.3 REFRESH

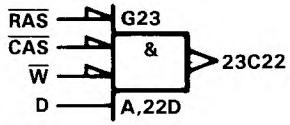
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required to carry out refreshing are not indicated by the symbol.

4.4 POWER DOWN



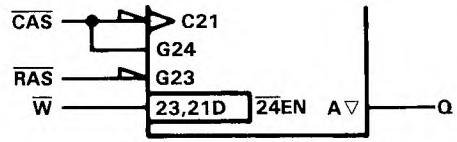
$\overline{CAS}$ is ANDed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

4.5 WRITE



By virtue of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ already low ($\overline{RAS}$ is ANDed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

4.6 READ



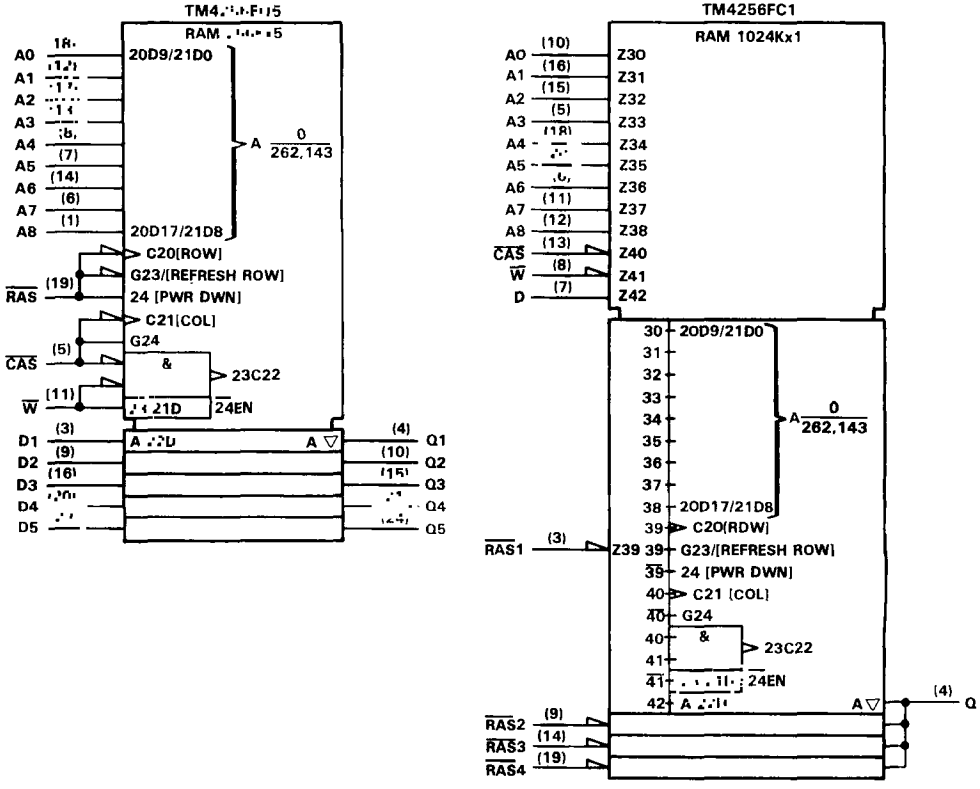
The ANDed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be a "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be ANDed with the output of the latch (by G24 and $\overline{24}$). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

5. SYMBOLS FOR DYNAMIC RAM MODULES

A dynamic RAM module is created by attaching separate DRAMs in chip-carrier packages to a common substrate. The symbols for the composite memory thus created starts with the symbol for the original DRAM and is used with as little change as possible.

So far, two types of organizations have evolved. In the first, all like address and control inputs are connected in parallel between the separate packages. Taking the TM4256EQ5 as typical of this group, the symbol starts with that of the TMS4256 with the qualifying symbol changed from "RAM 256K x 1" to "RAM 256K x 5", and this becomes a common control block for an array of five input-output elements shown below it.

In the second type of organization, of which the TM4256FC1 is typical, most of the address and control lines are parallel connected, but some are brought out separately for each of the DRAM packages. In order to maintain the recognizability of the original TMS4256 symbol, it has now been placed in the first element of the array. The empty rectangles located below the first element represent three other identical elements. Now interconnection (Z) dependency has been used (see 2 and 2.1) to show how CAS, W, D, and the address inputs connect to the first element, and since these inputs are located in the common control block, the connections apply equally to all the elements. The connections for $\overline{RAS}1$, $\overline{RAS}2$, $\overline{RAS}3$, and $\overline{RAS}4$ apply only to the individual elements.



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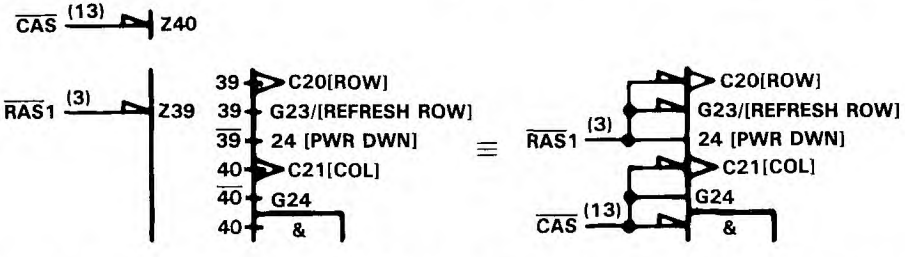
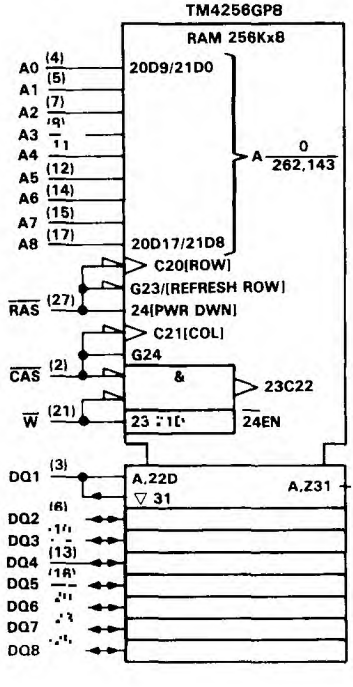
The drawings below illustrate the handling of control lines that in the original symbol were broken up into active-high and active-low functions. To make the combined symbol, the one of the two levels that seemed most appropriate was chosen, and then bars were used over the dependency numbers if necessary. For example, PWR DWN is an active-high function of pin 3, but it was decided that pin 3, $\overline{RAS}$, should be considered active low. The bar over the number 39 indicates that PWR DWN is a function of the *complement* of Z39 (ANDed with the complement of Z40 through G24), and the complement of active low is active high.



Another modification of the basic symbols that can occur in either organization is illustrated by the TM4256GP8. The TMS4256 has separate input and output pins. In the module, these have been connected together to form a single I/O port. In the module symbol, this is indicated using Z dependency to transfer the output signal from the right side to the left side.



If you have questions on this Explanation of IEEE/IEC Logic Symbols, please contact:

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